

REMARKS

Claims 1-48 are pending in the application of which claims 13-24 and 37-48 are withdrawn from consideration. Claims 1-12 and 25-36 are rejected.

Claims 1-8, and 25-32 were rejected under 35 USC 103(a) as being unpatentable over Itazu in view of Fujine. Claims 9-12 and 33-36 were rejected under 35 USC 103(b) as being unpatentable over Itazu in view of Fujine and in view of Djaja. Claims 1 and 25 include “...generating a model of said module by replacing each of said plurality of transistors in said topology by a corresponding one of a plurality of current sources ...”. The references of record do not show, teach, or suggest the above recited limitations of claims 1 and 25. The Fujine reference does not disclose replacing each transistor with a current source. Fujine only discloses that “circuit elements, such as transistors, logic gates and functional blocks, are converted to current sources based on design information stored in the design information storage means”. Fujine does not disclose that each transistor is replaced by a corresponding current source. There is nothing in Fujine that teaches how each individual transistor would be replaced by a corresponding current source. Therefore, combining Itazu with Fujine does not teach the above recited limitations of claims 1 and 25. Also, the references do not show, teach, or suggest “computing a magnitude of each of said plurality of current sources by distributing an aggregate amount of current sunk by said module among said plurality of current sources”. Claims 2-12 depend from claim 1. Claims 26-36 depend from claim 25. Therefore, claims 1-12 and 25-36 are believed to be allowable over the references of record.

It is believed that the above remarks are fully responsive to the Official Action. Reconsideration and allowance are therefore respectfully requested.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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